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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/868,322	06/18/2001	Yojiro Matsueda	109503	9116

25944 7590 05/17/2006

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EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/868,322	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Jennifer T. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-37,45,46,49,51 and 53-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-37,46,49,51 and 53-60* is/are rejected.

7)☒ Claim(s) *45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 12/30/2005.

Claim Objections

2. Claim 27 is objected to because of the following informalities: the limitation "*second image signals* that are generated by *digital to analog conversions*... supplied to *one data line*" is improper. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 27-32, 35, 37, 46, 49, 51, 53-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Quanrud (U.S. Patent No. 6,339,417) and further in view of Sasaki (U.S. Patent No. 6,049,321).

Regarding claim 27, referring to Figs. 1B, 15, 47A and 47B, Ikeda teaches a display device, comprising:

a display section (132) having a plurality of scanning lines (137) and a plurality of data lines (136) formed in a grating form corresponding to dots (138) as minimum units of display and active elements provided corresponding to intersections (Fig. 1B, col. 9, line 62 to col. 10, line 8);

a scanning line driver (130) that selects and drives the scanning lines (137);

a data line driver (not shown) that drives the plurality of data lines (136);

a memory (2425) (Fig. 47A) having a plurality of memory cell groups (hex0,hex0-hex0,hexEF) that include the plurality of memory cells being arranged in a matrix having a plurality of rows and a plurality of columns (Fig. 15, col. 10, lines 38-44);

a selection switch section (2423) that controls transmission of an image signal to the plurality of memory cell groups, each of the plurality of memory cell groups including memory cells, the memory cell section being disposed between the display section and the selection switch (col. 33, line 55 to col. 34, line 17),

each of the plurality of memory cell groups storing first image signals supplied through the selection switch section, and

second image signals that are generated based on the first image signals being supplied to one data line of the plurality of data lines (col. 34, lines 28-65).

Ikeda differs from claim 27 in that he does not specifically teach the display section, the memory, and the column selection switch section being formed on one substrate.

Quanrud teaches display section, selection switch section and the memory being formed on one substrate (col. 5, lines 12-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the display section, the memory, and the column selection switch section being formed on one substrate as taught by Quanrud in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced.

The combination of Ikeda and Quanrud differs from claim 27 in that it does not specifically teach the second image signals that are generated by digital to analog conversions.

Sasaki teaches image signals that are generated by plurality of DACs (34) being supplied to data lines (fig. 1, col. 5, lines 6-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the image signals that are generated by digital to analog conversions as taught by Sasaki in the system of the combination of Ikeda and Quanrud in order to create analog signals to data lines of the matrix display.

Regarding claims 28, 49, and 51, Ikeda further teaches the memory cell section (2425) storing image signals for one screen (2451) (Fig. 1, 15, 17A, and 17B, from col. 31, line 40 to col. 33, line 67).

Regarding claim 29, Ikeda further teaches a plurality of word lines among which a word line is selected when a memory cell of the plurality of memory cells receives the image signal, the plurality of word lines extending along a row direction that intersects a column direction along which the plurality of data lines extend (Fig. 1A and 15).

Regarding claims 30-31, Ikeda further teaches on the basis of an address signal representative of a display position and a storage position, said scanning line driver selects the scanning lines and the word line driver selects said word lines (Fig. 1A, col. 9, lines 19-67).

Regarding claims 32, 54, and 55, the combination of Ikeda, Quanrud and Sasaki teaches a DAC section having a plurality of DACs (34), each of the plurality of DACs receiving digital data based on the image signal, each of the plurality of DACs converting the digital data into analog data (col. 5, lines 6-9).

Regarding claim 35, Ikeda teaches only when a change of display in one dot of the plurality of dots is carried out, a memory cell of the plurality of memory cells that corresponds to the one dot receiving the first image signals (Figs. 17A and 17B) (col. 14, lines 13-49).

Regarding claim 37, the combination of Ikeda and Quanrud does not specifically teach the length of the matrix in a row direction extend being shorter than a length of the display. However, it is the matter of design choice to obtain the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction. Therefore, it would have been obvious to obtain the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction, in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced.

Regarding claim 46, Ikeda teaches a column decoder (112) that selects a memory cell of the plurality of memory cells by cooperation with the word line (Figs. 1A and 15) (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claim 53, Ikeda teaches a gray scale level in the display section being obtained by an area gray scale method (Fig. 21, col. 16, line 52 to col. 17, line 35).

Regarding claim 56, the combination of Ikeda, Quanrud and Sasaki teaches a sense amplifier section (35) (col. 4, lines 63-65 of Sasaki).

Regarding claim 57, although the combination of Ikeda, Quanrud and Sasaki does not specifically teach the DAC section being disposed between the sense amplifier section and the display section. However, it would have been obvious to obtain the DAC section being disposed between the sense amplifier section and the display section in order to provide the most efficient layout on the basic of establishing a driving circuit.

Regarding claim 58, Ikeda teaches a memory row decoder (2456) (Fig. 47A) for operating the plurality of memory cells (2425), the memory decoder and the scanning line driver

receiving a common controlling signal (i.e., the timing control signal from the timing control circuit 1610, Fig. 16, col. 10, lines 48-63) .

Regarding claim 59, the combination of Ikeda, Quanrud and Sasaki teaches the substrate being a glass substrate (col. 3, lines 65-67 of Quanrud).

5. Claims 33, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Quanrud (U.S. Patent No. 6,339,417) and Kumagai et al. (U.S. Patent No. 5,440,718).

Regarding claims 33, 34, and 36, the combination of Ikeda and Quanrud differs from claims 33, 34, and 36 in that it does not specifically teach the plurality of the memory cell section being configured by a dynamic memory. However, Kumagai teaches the plurality of the memory cell section being configured by a dynamic memory (col. from col. 3, line 64 to col. 4, line 18 of Kumagai). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the dynamic memory as taught by Kumagai in the system of the combination of Ikeda and Quanrud in order to refresh the data storage easily.

6. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136), Quanrud (U.S. Patent No. 6,339,417) in view of Plus et al. (Patent No. 5,170,155) and further in view of Yamazaki et al. (Patent No. 6,472,684).

Regarding claim 60, the combination of Ikeda, Quanrud and Plus differs from claim 60 in that it does not specifically teach each of the plurality of memory cells being formed of TFTs.

Yamayaki teaches each of the plurality of memory cells being formed of TFTs (col. 1, lines 54-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the memory cells being formed of TFTs as taught by

Yamayaki in the system of the combination of Ikeda, Quanrud and Plus in order to reduce the thickness of the memory, resulting in miniaturization of the device.

7. Claim 45 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Applicant's arguments with respect to claims 27-37, 46, 49, 51, and 53-58 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JNguyen
5/6/06

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